AMENDMENTS TO THE SPECIFICATION:

Please amend the caption at page 1, line 9, as follows:

BACKGROUND ~~OF THE INVENTION~~

Please amend the paragraph beginning at page 1, line 16, and continuing to page 1, line 21, as follows:

As a device is scaled ~~has~~ to become smaller, ~~and the~~an aspect ratio of a via hole in which a wire is buried in the device has accordingly increased~~,~~. Size reduction, however, can result in a problem of development of a void within the via hole ~~has arisen as a problem with~~when implementing ~~-~~a method of manufacturing an embedded multilevel interconnection which uses a conventional damascene process

Please amend the paragraph beginning at page 2, line 5, and continuing to page 2, line 12, as follows:

A displacement plating method can utilize~~s~~ that in a plating solution~~, w~~. When the oxidation-reduction potential of underlying metal is lower than the oxidation-reduction potential of copper which is contained in the plating solution, ions of the underlying metal are oxidized and accordingly dissolve in the plating solution~~, and instead~~,. On the other hand, copper ions within the plating solution are reduced and deposited

Please amend the caption at page 5, line 1, as follows:

BRIEF SUMMARY ~~OF THE INVENTION~~

Please amend the paragraphs beginning at page 5, line 2, and continuing to page 5, line 22?, as follows:

~~An object of the present invention is to provide a~~A method of manufacturing a multilevel interconnection for an LSI having fine wires is provided, according to which a native oxide film formed on a surface of a barrier metal film is thin and development of a void is prevented.

The present ~~invention~~ technology is directed to a method of manufacturing an embedded multilevel interconnection, comprising: a step of forming a hole portion in an insulating layer; a barrier metal film forming step of forming a barrier metal film mainly made of tantalum and nitrogen in such a manner that the barrier metal film covers at least an inner wall of the hole portion, an element composition ratio (N/Ta) of nitrogen to tantalum contained in the barrier metal film being 0.3 or higher but 1.5 or lower; a removal step of removing an oxide film formed on a surface of the barrier metal film; and an electroless plating step of immersing the barrier metal film in a plating liquid comprising copper and thereby forming an electroless copper plating film on the barrier metal film.

Please amend the paragraph beginning at page 6, line 22, and continuing to page 7, line 6, as follows:

The present ~~invention~~ technology may further contain a step of plating an electrolytic copper plating film on the electroless copper plating film by using the electroless copper plating film as a seed layer.

As clearly described above, by using the method of manufacturing a multilevel interconnection according to ~~the present invention~~an example embodiment, growth of a native oxide film on a surface of a barrier metal film is suppressed. This makes it possible to form a buried interconnection in which development of a void is discouraged.

Please amend the paragraph beginning at page 7, line 9, and continuing to page 7, line 11, as follows:

FIGS. 1A-1E shows cross sectional views of the steps of manufacturing a multilevel interconnection according to ~~the~~ an example embodiment ~~1 of the present invention~~;

Please amend the paragraphs beginning at page 7, line 24, and continuing to page 8, line 9, as follows:

FIG. 1 shows cross sectional views of steps of manufacturing a multilevel interconnection according to an example embodiment ~~1~~. In FIG. 1, the same reference symbols to those shown in FIG. 3 denote the same or corresponding portions. These manufacturing steps include the following ~~steps~~ acts 1 through 5.

~~Step~~ Act 1: As shown in FIG. 1A, an inter-layer insulating film 3 of silicon oxide is formed on an inter-layer insulating film 1 which is made of silicon oxide and has a lower-layer wire 2. Next, the inter-layer insulating film 3 is etched, thereby forming a via hole (hole portion) 4.

Please amend the paragraph beginning at page 9, line 22, and continuing to page 10, line 4, as follows:

~~Step~~ Act 2: As shown in FIG. 1B, the barrier metal film 5 is exposed to atmosphere, whereby the surface of the barrier metal film 5 is oxidized and the native oxide film 6 of TaN is formed. At this stage, the element composition ratio (N/Ta) of the barrier metal film 5 is controlled to be 0.3 or higher but 1.5 or lower. Hereby, the film thickness of the native oxide film 6 formed by oxidation of the barrier metal film 5 is about 1 nm or thinner.

Please amend the paragraph beginning at page 10, line 11, and continuing to page 10, line 18, as follows:

~~Step~~ Act 3: As shown in FIG. 1C, the native oxide film 6 formed on the surface of the barrier metal film 5 is removed by etching. The etching uses a mixture of a hydrofluoric acid and a nitric acid or a diluent which is prepared by diluting a hydrofluoric acid with pure water ten or more times. This makes it possible to selectively remove the native oxide film 6 without damaging the barrier metal film 5.

Please amend the paragraph beginning at page 11, line 2, and continuing to page 11, line 9, as follows:

~~Step~~ Act 4: As shown in FIG. 1D, by means of immersion into a plating liquid which contains copper, electroless plating is executed. The plating liquid is mainly made of copper sulfate, a glyoxylic acid (reducer), ethylene diaminetetraacetate (complexing agent) and bipyldin (stabilizer). Plating conditions are, for instance, that pH of the solution is 12 and the temperature of the solution is 70^0C.

Please amend the paragraphs beginning at page 11, line 19, and continuing to page 11, line 25, as follows:

~~Step~~ Act 5: As shown in FIG. 1E, by an electrolytic plating method, an electrolytic copper plating film 8 is formed. The electrolytic plating uses a solution which is mainly made of copper sulfate.

Through these ~~steps~~acts, a multilevel interconnection 100 is obtained whose via hole 4 is filled up with copper without any void as shown in FIG. 1E.

Please amend the paragraph beginning at page 12, line 2, and continuing to page 12, line 8, as follows:

A method of manufacturing a multilevel interconnection according to the embodiment 2 of the present invention is different as for the step of forming the barrier

metal film 5 (~~step~~ act 1) from but is otherwise similar to the manufacturing method according to the embodiment 1 described above.

Please amend the paragraph beginning at page 13, line 13, and continuing to page 13, line 15, as follows:

As the ~~steps~~ acts 3 through 5 shown referred to for the embodiment 1 (FIGS. 1C-1E) are carried out after this, the multilevel interconnection 100 is obtained.